CLAIMS

1. (Currently Amended) A receiver, comprising:

a latching mechanism, coupled to receive a data stream comprising a plurality of data units and to receive a plurality of latching control signals, each data unit occupying a data period, said latching mechanism latching said data units in response to said latching control signals;

a signal generator coupled to receive a reference signal, said signal generator generating said plurality of latching control signals ~~based upon~~ responsive to said reference signal, where the plurality of latching control signals are offset; and

an adjustable delay element coupled to receive a clock signal and delaying said clock signal according to a phase difference between said clock signal and said data stream ~~by a variable delay~~ to derive said reference signal, said reference signal so derived causing said signal generator to generate said latching control signals such that each of said latching control signals coincides approximately with a midpoint of a data period.

2. (Original) The receiver of claim 1, wherein said clock signal is synchronized with said data stream but is not necessarily aligned therewith.

3. (Currently Amended) The receiver of claim 1, wherein ~~said variable delay of~~ said adjustable delay element delays said clock signal ~~is~~ greater than or equal to said data period.

4. (Original) The receiver of claim 1, wherein there is no more than one of said latching control signals per data period.

5. (Currently Amended) The receiver of claim 1, further comprising:

a delay control mechanism, said delay control mechanism adjusting ~~said variable delay imposed by~~ said adjustable delay element to alter said reference signal, said reference signal being so altered to cause said signal generator to generate said latching control signals such that each of said latching control signals coincides more closely with a midpoint of a data period.

6. (Original) The receiver of claim 5, wherein said delay control mechanism alters said reference signal by causing said reference signal to coincide more closely with a midpoint of a data period.

7. (Original) The receiver of claim 6, wherein at least one of said latching control signals is delayed relative to said reference signal by substantially a data period.

8. (Original) The receiver of claim 7, wherein each of said latching control signals is temporally separated from another latching control signal by substantially one data period.

9. (Original) The receiver of claim 8, wherein said signal generator comprises a delay locked loop.

10. (Currently Amended) The receiver of claim 5, wherein said delay control mechanism comprises:

a detection mechanism, said detection mechanism receiving an indication of how closely each of said latching control signals coincides with a midpoint of a data period, and providing an adjustment signal to adjust ~~said variable delay of~~ said adjustable delay element

to alter said reference signal to cause each of said latching control signals to coincide more closely with a midpoint of a data period.

11. (Original) The receiver of claim 10, wherein said delay control mechanism further comprises:

a fixed delay element coupled to receive at least one of said latching control signals and providing a delayed latching signal; and

a latching component coupled to receive said data stream, said latching component latching one of said data units in said data stream in response to said delayed latching signal.

12. (Previously Presented) The receiver of claim 11, wherein said detection mechanism receives said one data unit from said latching component, and compares said one data unit with a plurality of data units received from said latching mechanism to determine how closely each of said latching control signals coincides with a midpoint of a data period.

13. (Original) The receiver of claim 12, wherein said fixed delay element has a fixed delay greater than said data period.

14. (Original) The receiver of claim 13, wherein said fixed delay is approximately (X+.5) times said data period where X is an integer greater than or equal to 1.

15. (Original) The receiver of claim 12, wherein said detection mechanism comprises a phase detector.

16. (Currently Amended) ~~The~~ A receiver comprising: ~~of claim 1, wherein said signal generator comprises a delay locked loop~~.

a latching mechanism, coupled to receive a data stream comprising a plurality of data units and to receive a plurality of latching control signals, each data unit occupying a data period, said latching mechanism latching said data units in response to said latching control signals;

a signal generator including a delay locked loop coupled to receive a reference signal, said delay locked loop generating said plurality of latching control signals responsive to said reference signal, where the latching control signals are offset by substantially one data period; and

an adjustable delay element coupled to receive a clock signal and delaying said clock signal according to a phase difference between said clock signal and said data stream to derive said reference signal, said reference signal so derived causing said delay locked loop to generate said latching control signals such that each of said latching control signals coincides approximately with a midpoint of a data period.

17. (Original) The receiver of claim 16, wherein there is no more than one of said latching control signals for each of said data periods.

18. (Original) The receiver of claim 16, wherein said reference signal coincides approximately with a midpoint of a data period.

19. (Original) The receiver of claim 5, wherein at least one of said latching control signals is delayed relative to said reference signal by substantially one data period.

20. (Original) The receiver of claim 19, wherein each of said latching control signals is temporally separated from another latching control signal by substantially one data period.

21. (Currently Amended) A receiver, comprising:

a latching mechanism, coupled to receive a data stream comprising a plurality of data units and to receive a plurality of latching control signals, each data unit occupying a data period, said latching mechanism latching said data units in response to said latching control signals; and

a signal generator coupled to receive a reference signal which is not aligned with said data stream, said signal generator generating said latching control signals based upon said reference signal such that each of said latching control signals coincides approximately with a midpoint of a data period, where the latching control signals are offset by substantially one data period.

22. (Original) The receiver of claim 21, wherein there is no more than one of said latching control signals for each of said data periods.

23. (Original) The receiver of claim 21, wherein said reference signal coincides approximately with a midpoint of a data period.

24. (Original) The receiver of claim 23, wherein said reference signal is derived by delaying a clock signal, which is synchronized and aligned with said data stream, by a delay which is approximately equal to (X+.5) times said data period where X is an integer greater than or equal to 1.

25. (Original) The receiver of claim 23, wherein at least one of said latching control signals is delayed relative to said reference signal by substantially one data period.

26. (Original) The receiver of claim 25, wherein each of said latching control signals is temporally separated from another latching control signal by substantially one data period.

27. (Original) The receiver of claim 26, wherein said signal generator comprises a delay locked loop.

28. (Currently Amended) A receiver comprising:

a latching mechanism, coupled to receive a data stream comprising a plurality of data units and to receive a plurality of latching control signals, each data unit occupying a data period, said latching mechanism latching said data units in response to said latching control signals; and

a delay locked loop coupled to receive a reference signal, said delay locked loop generating said latching control signals ~~based upon~~ responsive to said reference signal such that each of said latching control signals coincides approximately with a midpoint of a data period, where the reference signal is a variably delayed signal and where each of the latching control signals are offset by substantially one data period.

29. (Original) The receiver of claim 28, wherein there is no more than one of said latching control signals per data period.

30. (Original) The receiver of claim 28, wherein said reference signal is not aligned with said data stream.

31. (Original) The receiver of claim 30, wherein said reference signal coincides approximately with a midpoint of a data period.

32. (Original) The receiver of claim 31, wherein said reference signal is derived by delaying a clock signal, which is synchronized and aligned with said data stream, by a delay which is approximately equal to (X+.5) times said data period where X is an integer greater than or equal to 1.

33. (Original) The receiver of claim 31, wherein at least one of said latching control signals is delayed relative to said reference signal by substantially one data period.

34. (Original) The receiver of claim 33, wherein each of said latching control signals is temporally separated from another latching control signal by substantially one data period.